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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,413	11/10/2003	Hiroyuki Morishita	82478-1800	5180

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,413	MORISHITA ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on June 19, 2006. This amendment has been entered and carefully considered. Claims 1, 14 and 15 are amended and claims 8-9 are cancelled. Therefore, claims 1-7 and 10-17 are pending in this application.

2. Applicant's arguments with regards to claims 1-7 and 18 filed on March 15, 2005 have been fully considered but they are not deemed to be persuasive in view of new grounds of rejection.

Claim Rejections - 35 USC § 103

3. Claims 1-3, 10-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy ("The Cache Memory book") in view of Suh et al. ("Dynamic Cache Partitioning for Simultaneous Multithreading Systems") further in view of Chiou et al. (USPN: 6,370,622) hereinafter, Chiou.

Regarding claims 1, and 14-17, Handy shows that a computer with a cache, main memory, a microprocessor, an address receiving unit, a caching unit to acquire the data block from main memory (pg 12, 51, and 52), having the address converting unit convert the logical address to the physical address, sending the address to the receiving unit, and storing the physical address in the cache were well known in the art (pg 12 and 52). Furthermore, Handy further shows an address receiving unit to receive a logical address, a data block managing unit to manage data stored in the cache using

the logical addresses, and an address converting unit to convert the address to the physical address and sent it to main memory (pg 12 and 52). However, Handy does not expressly show a region-managing unit to manage regions in the cache. Suh et al. does teach the use of a region-managing unit that manages regions in cache. Handy and Suh et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow for dynamic partitioning. The suggestion for doing so would have been to increase cache performance. Therefore, it would have been obvious to combine Suh et al. and Handy for the benefit of a more efficient cache to obtain the invention as specified in claims 1 and 14-17.

However, none of them are teaching the further limitation of having a judging unit as claimed. Chiou, on the other hand, teaches about judging whether the requested data is stored in the cache memory by searching all of the plurality of regions in the cache memory (i.e. by searching all the column caches when the cache miss occurs) (e.g. see Col. 18, lines 1-24). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the judging function taught by Chiou in the cache controller taught by the combination of Handy and Suh. In doing so, the number of cache miss is reduced by getting the cache hit for the requested data not present in the requesting column cache (i.e. the cache region) but present in any other column cache within the entire cache. Therefore, the performance of the computer system increases.

Regarding claims 2 and 3, Suh et al. goes on to further describe that the region managing unit divides the cache into a plurality of regions equal to the number of tasks and finds out how many tasks are running and divides the cache based on the information. Handy and Suh et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow for these features of dynamic partitioning. The suggestion for doing so would have been to increase cache performance. Therefore, it would have been obvious to combine Suh et al. and Handy for the benefit of a more efficient cache to obtain the invention as specified in claims 1 and 14-16.

Regarding claims 10-11, the combination of Handy and Suh teaches the claimed invention as described above and furthermore, Handy discloses that the cache memory is made of a plurality of ways, and the plurality of regions each contain at least one way. Handy also teaches about using set associative mapping for each region containing more than one way (e.g. see pgs 53-55).

Regarding claims 12 and 13, Handy, Chiou and Suh et al. describe all the limitations of claim 1 and furthermore. Chiou discloses a region management unit that divides the cache into specific regions and nonspecific regions, manages the specific regions in correspondence w/ a specific task where the caching unit stores the acquired data into the specific region if the task is a specific task, a microprocessor that executes tasks where a region management unit divides the cache into two regions, the first region holds a first and second task while a second region holds a third task, and the

caching unit stores the acquired data blocks into the region in cache that they are supposed to go (e.g. see Col. 18, lines 1+). Handy, Suh et al.. and Chiou are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to divide up the cache into multiple regions. The suggestion for doing so would have been to correctly separate data. Therefore, it would have been obvious to combine Handy, Suh et al., and Chiou for the benefit of a more efficient cache to obtain the invention as specified in claims 12 and 13.

4. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al. and Chiou as applied to claims 1-3 above, and further in view of Patterson et al.

Regarding claim 4, Handy, Suh et al. and Chiou described all of the limitations of claims 1-3 and Suh et al. further describes having the region management unit managing a plurality of regions in a one-to-one correspondence with task (process) identifiers. Neither of Handy, Suh et al. and Chiou expressly describe a task identifier unit to receive task identifiers or a caching unit that stores acquired data blocks in the cache corresponding to the received task identifier. Patterson et al. does describe a task identifier unit to receive task identifiers or a caching unit that stores acquired data blocks in the cache corresponding to the received task identifier. Handy, Suh et al., Chiou and Patterson et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to

a person of ordinary skill in the art to attach task identifiers to data in the cache. The suggestion for doing so would have been correctly separate and earmark data. Therefore, it would have been obvious to combine Patterson et al., Suh et al. and Handy for the benefit of classification to obtain the invention as specified in claim 4.

Regarding claim 7, Patterson et al. shows that the task identifier could be a process identifier assigned and ran by the operating system (pg 598) and evidentiary support shows that a microprocessor that could perform multitasking under the control of an operating system for a while (Review of operating systems). Handy, Suh et al., Chiou and Patterson et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to attach task identifiers to data in the cache. The suggestion for doing so would have been correctly separate and earmark data. Therefore, it would have been obvious to combine Patterson et al., Suh et al., Chiou and Handy for the benefit of classification to obtain the invention as specified in claim 7.

5. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al., Chiou and Patterson et al. as applied to claims 1-4 above, and further in view of Thaler et al. (Pat No 5983329).

Handy, Suh et al., Chiou and Patterson et al. describe all the limitations given in claims 1-4, but do not expressly disclose the task identifier being an address of the data location in main memory. Thaler et al. does describe the task identifier being the address of the data location in main memory (column 4, lines 38-46). Handy, Suh et al.,

Chiou, Patterson et al. and Thaler et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the task identifier be the address of the data in main memory. The suggestion for doing so would have been to save cache space while still uniquely identifying all data in the cache. Therefore, it would have been obvious to combine Handy, Suh et al., Chiou, Patterson et al. and Thaler et al. for the benefit of saved space to obtain the invention as specified in claim 5.

6. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al., Chiou and Patterson et al. as applied to claims 1-4 above, and further in view of Hum et al. (Pub No 20020087824).

Handy, Suh et al., Chiou and Patterson et al. describe all the limitations given in claims 1-4, but do not expressly disclose that the task identifier is generated by converting an address of a location in the main memory at which the task is stored as a program. Hum et al. does disclose the task identifier is generated by converting an address of a location in the main memory at which the task is stored as a program (paragraph 16). Handy, Suh et al., Chiou, Patterson et al. and Hum et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the task identifier be a derivation of the address of the data in main memory. The suggestion for doing so would have been to have a unique identifier for each set of data

in the cache while still being able to extract the address of the data in main memory and thus saving space. Therefore, it would have been obvious to combine Handy, Suh et al., Chiou, Patterson et al. and Hum et al. for the benefit of space saving to obtain the invention as specified in claim 6.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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